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Novel Techniques for Millimeter Wave Packages

Martin Herman, Karen Lee, Lynn Lowry, Elzbieta Kolawa, Ann Tulintseff

Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive (m/s 161-213)
Pasadena, CA 91109

Fax. (818) 393-6875

Abstract

A new millimeter-wave package architecture with supporting electrical, mechanical and material science experiment and analysis is presented. This package is well suited for both individual devices/MMICs and multichip module (MCM) applications. It also has low-loss wideband RF transitions which are necessary to overcome manufacturing tolerances which leads to lower per unit cost. Novel applications of this new packaging architecture which go beyond the standard requirements of device protection include: integration of antennas, compatibility to photonic networks and direct transitions to waveguide systems are described.

Techniques for electromagnetic analysis, thermal control and hermetic sealing were explored. 3D electromagnetic analysis was performed using the Finite-Difference Time-Domain (FDTD) algorithm and experimentally verified for millimeter-wave package input and output transitions. Novel multi-material system concepts which allow excellent surface finishes to be obtained (reducing RF loss) and enhance thermal management (AlN, Cu, and diamond thin films) have been investigated. A new approach utilizing block copolymer coatings was employed to hermetically seal packages which met MIL STD-883.

I. Introduction

Millimeter-wave systems for commercial, NASA deep space communication, and DoD applications are rapidly emerging; therefore, high frequency packaging technology for individual devices and multi-chip components which provide excellent electrical/mechanical performance and is affordable will be required. The latter characteristic was named as a major challenge at the Special Technology Area Review (STAR) on Microwave Packaging [1].

This article describes the key characteristics of a new package architecture [2-4] which is shown in Figure 1. Section II describes the package concept in more detail. We address the design, fabrication and testing of the external package interconnects and the mechanical/material composition of our new package including novel concepts for multi-material (alumina, aluminum nitride (AlN) and copper) substrates with smooth surface finishes and high thermal spreading capability. We also describe a simple yet effective hermetic sealing method using a block copolymer coating that was tested on standard Ku-Band packages. We conclude with a brief description of novel applications of our basic package architecture and summary of results in Sections III and IV, respectively.

A. Future Spacecraft Needs

Potential future JPL / NASA missions (such as: Pluto Fast Flyby, Small Solar Probe, Mars Surveyor Program, and The Discovery Series etc.) are minimizing spacecraft mass in order to accelerate mission plans and reduce costs by using smaller launch vehicles. Electronic packaging accounts for up to 30% of the overall spacecraft mass and the use of high density packaging is necessary to achieve mass and volume reduction goals in order to enable the use of Pegasus and Delta 11 launch vehicles, for example. Consequently, advanced high density electronic packaging has been identified as a high priority technology need in the near term by JPL pre-projects.

Driving forces for miniaturization and increased science return have influenced telecommunication system and hardware designers to use high density packaging technologies and to employ X- and Ka-Band frequencies to enhance mission data rates. High frequency packaging can reduce telecommunication subsystem mass as much as 40% [5].

During our concurrent development of a 32 GHz high power solid state power amplifier (SSPA) for spacecraft transmitters and a 30 GHz active array for the Advanced Communications Technology Satellite (ACTS) Mobile Terminal we found, after talking with over 50 different US and European companies, that we could not purchase an existing commercial package. This provided our prime motivation for the development of a manufacturable Ka-Band package. Due to limited funding, we concentrated on the development of new techniques such as package architecture, 3-D electromagnetic analysis, and material composition with the intent that our solutions could be easily transferred to industry to overcome this lack of availability. In fact, only recently have "commercial" packages been developed which can break the 30 GHz barrier [6,7],

B. High Density Packaging and Key Characteristics

Microelectronic packaging provides four basic functions [8]:

- Power distribution
- Signal distribution
- Heat dissipation
- Environmental protection.

High density electronic packaging refers to the incorporation of multiple integrated circuits, as bare die and passive components on a common interconnecting substrate. This format is commonly referred to as a multichip module (MCM). Significant improvements in circuit density are attainable (10-30 times), as compared with printed circuit board technology. Mass/volume reductions of 75% for advanced spaceborne computers using high density packaging technologies have been demonstrated,

For high-density high-frequency (1 GHz to 100 GHz) packages, the performance requirements of the aforementioned list are more stringent. Signal distribution becomes a major challenge as the frequency and packaging densities increase. Stray (RF) radiation in the form of crosstalk and package moding become limiting factors which must be addressed in order to preserve performance. The interconnecting networks into and out of the package must have low loss characteristics and be impedance matched to the adjacent networks. 3-D high density formats which use multilayer material systems and embedded components further complicate signal propagation characteristics and thermal management issues.

Any packaging technology development for devices/MMICs should be capable of being converted into an MCM. This is where high-density packaging is most effective in reducing cost and subsystem mass/volume.

11. Package Description

A. First and Second Level Packaging

A hierarchy of packaging levels has been established, Packaging at the chip/device interconnect regime is considered at level 1. The housing and external interconnection of the package are at level 2. As we. try to miniaturize and simplify the package design, levels 1 and 2 merge together. First level packaging involves die and substrate attach and interconnect methods. For low frequency electronics, many different methods have been developed for multichip modules (wire-bond, tape-automated bond, bump bond, chip-first with interconnects to the host substrate deposited on top, and others). There are man y options and the tradeoffs at the early design phase which strongly influence the final module cost [9]. At higher frequencies, the methods are not yet as exotic, primarily limited to eutectic or epoxy substrate and die attach and wire-bond interconnects. Some flip chip microwave components are available from certain foundries. The package topology proposed would be able to accommodate all the various low and high frequency first level interconnection schemes.

The second level is the traditional outer housing, what most microwave system engineers think of when taking about packaging, Traditionally millimeter-wave planar circuits are embedded in a below-cutoff channel where a stripline to waveguide transition is employed and a hermetic waveguide window seal ensures complete closure. An alternate approach is to use a stripline-to-coaxial glass bead which provides a hermetic transition. As millimeter-wave circuits shrink with further integration, the housing and transitions be.come the limiting factors in reducing mass and “” volume of the component. Furthermore, for high frequencies the tight mechanical tolerances required drive up traditional package manufacturing costs [1].

With the onset of Monolithic Microwave Integrated Circuits (MMICs), there have been a few efforts to provide generic packages [10- 14]. Many of these employed a microstrip-stripline-microstrip transition into and out of the package. The version made from quartz substrates had very low loss, however achieving hermeticity was a problem and work has stopped in this area. Most recently, alumina packages with very low insertion loss (0.6 dB) has been reported. Unfortunately, these packages are not commercially available. In another case, if a package or cavity size requires modification, a large non-recurring charge is involved with at least a year wait before delivery.

B, Topology and Manufacturability

A package concept under development at JPL [2] addresses the needs of a compact, hermetic, low loss package for low and medium power (<3W dissipated) millimeter-wave devices and MMICs. It is comprised of a multilayer planar circuit structure where the input and output RF signal paths are in microstrip. A microstrip topology was selected for ease of interconnection to MMICs and discrete devices inside the package and to a microstrip embedding networks outside (although many other planar transmission line media are compatible with the package architecture), The foundation of the package, called the structural substrate, is the base onto which devices and signal distribution circuits are mounted (Figure 2a). It provides the ground plane for the microstrip input / output (I/O) and a means for attachment of a package cover for hermetic sealing. Besides being the key for structural support, the structural substrate significantly affects thermal management and RF signal flow (Figure 2b). Its material may be metal, metallized dielectric, metal matrix, or new thin film high conductivity multilayer films on ceramics depending on the requirements for thermal management [15]. The J/O RF signals couple through apertures in the ground plane fabricated on the structural substrate (Figure 2c). These l/O transitions are broadband which eases fabrication tolerances to make the package readily manufacturable with standard hybrid microcircuit processes.

Interconnecting circuits, other active or passive devices, or even drop-in carriers can all mount to the structural substrate. Figure 2 depicts simple package concepts to house a single device; however the planar, multilayer package topology will readily adapt to a multichip module (MCM), where the interconnecting circuits can be realized by either conventional multilayer printed circuit technology (e. g. LTCC), or other advanced high density interconnect technology,

C. Electrical design of transitions

The standard microstrip-stripline-microstrip transition inherently has two physical discontinuities thereby creating the potential for high radiation and loss at millimeter-wave frequencies. The approach taken in our design was to use vertical interconnects through a ground plane. An elegant physical model of this transition based on a Green's function analysis is presented in [16] for an X-Band geometry, In our work bandwidth in excess of 10 GHz were measured on an alumina prototype. Early work on microstrip vertical interconnections is traceable to direct line-to-line couplers [17-20]. For packaging applications there is a need for ground plane continuity and shielding as well, which suggests a vertical transition from microstrip line through an aperture in its ground plane, to an inverted microstrip line beneath the common ground plane. Most work in this area has been applied to couplers and feeds for antennas [16, 21-27]. Simulations clearly show that very efficient wideband transitions are quite feasible and this has been verified experimentally in [16] and [24]. In this work, we extend the useful applications of this type of vertical interconnect to packaging, where circuit densities increase, and three-dimensional space needs to be considered. Based on the past published work, a rectangular aperture seems to be the best geometry to employ, Circular geometries seem to be better suited for low coupling applications [25],

Computer-aided analysis using two different techniques was used to determine the optimum design of the RF transition. The first was a commercial 2.5-D electromagnetic simulator (EM™, a product from Sonnet Software). The second was a Finite-Difference Time-Domain (FDTD) code developed at JPL [28] which runs on the JPL Cray Y-MP Supercomputer. Both electromagnetic simulation tools are easy to use. The three-dimensional FDTD method is a general, straight-forward implementation of Maxwell's equations and provides for the rigorous solution" of a variety of electromagnetic wave problems [29,30]. Recent work demonstrating the method's usefulness in analyzing microstrip circuit and antenna configurations complements the published literature in this area [28], In our development, we used an orthogonal grid with the choice of first and second order absorbing boundary conditions for the grid terminations. Frequency-dependent circuit and scattering parameters were obtained by taking the Fourier transform of time-domain quantities and then taking the proper ratios.

Since the FDTD method is carried out in the time-domain, it is amenable for use in solving configurations containing nonlinear devices. In fact, more recent work with the FDTD method has extended its use to include both passive and active lumped element devices, where the electric and magnetic fields are determined by satisfying the FDTD difference equations and the i-v characteristic of the device, We are currently working towards applying the FDTD method to analyze MMIC packages, both the passive aspects of the package, i.e., the transitions and overall configuration, and the effects of the package on the active component performance.

Sonnet's EM™ gave very good results for predicting trends and sensitivities with changes in the printed geometry. The FDTD code, however, produced a more accurate result in modeling a partially enclosed transition (see Figure 3). This is not surprising, nor does it mean that EM™ is inferior. The difference in the two methods lies in the formulation and geometry. In the FDTD code, properly placed conducting planes and absorbing boundary conditions are used to simulate our open package geometry. In EM^{TM} unbounded or open planes are simulated by invoking absorbing layers , therefore the walls containing the input and output ports remain defined as conductors.

To analyze our geometry (Figure 2a) we divided the package in half to decrease the overall computation time. By cascading the S-parameter results for two single transitions we are able to analyze a full back-to-back transition test structure. We excited the input transition via an open microstrip configuration into a shielded microstrip environment. For the sake of completeness we performed another analysis of a shielded microstrip excitation transition to an open microstrip line. ‘he calculated networks were cascaded together to give the overall package characteristics. We could have simply inverted the first transition's input/output ports via S-parameter manipulation and cascaded it to the original network to come up with a similar results. For a single transition, our FDTD analysis employed a time step of O. lps and spatial steps of 0.0508 mm, 0.0635 mm, and 0.0508mm in the x,y,z directions, respectively in order to maintain numerical stability and to achieve sufficient accuracy up to 50 GHz. The total number of cells was 101, 201, and 61 in the x, y, and z directions, respectively. The CPU time required for the calibration line (using a smaller grid) took 815.2s, the transition analysis 1092s and the Fourier transformation and S- parameter conversion 9.2s on JPL's Cray YMP. For comparison, Sonnet's EM^{TM} required roughly 2400s per frequency point for an identical structure comprised of 2030 subsections, run on a Sun Sparcstation2. EM^{TM} was used very effectively to optimize geometric parameters at a specific frequency of interest, and FDTD was used to determine the broadband response,

The performance of the RF transition is a function of several parameters. Our initial design was determined by varying the length of the microstrip open stub and the width and length of the coupling aperture (rectangular slot in the ground plane). Transmission and reflection as a function of stub length and slot width and length were calculated using EM™. The results of these analyses are plotted in Figure 4. The insertion and return loss at 32 GHz are not significantly affected by changes in these physical parameters which means alignment is less critical and the transition can tolerate fabrication errors less than several roils. Note that the response can be optimized at a single frequency for many combinations of stub and slot length, but the upper and lower cutoffs for the passband will shift. The transition is well suited for broadband applications and is extremely important for low cost manufacturing. The low frequency cutoff is determined by the lengths of the stub and slot. Figure 3 shows the simulation of a single transition for a 10 mil thick alumina to 10 mil thick alumina transition. Figure 5 shows good agreement between measured and modeled performance of our prototype back-to-back transition. At the higher end of the passband our measurement accuracy was degraded due to fixture mismatch, The work shown was a first pass design; thus, demonstrating the robustness and simplicity of the architecture for millimeter-wave applications.

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D. Substrate material requirements

The structural substrate must provide an efficient low impedance path for heat dissipation. One solution is to utilize a thick ground plane, e.g. copper or copper-tungsten (Figure 2b). However, this complicates the package structure and increases manufacturing costs. An alternative is to use a substrate which can easily spread heat to a thermal sink. In addition to excellent thermal properties the material must have a similar thermal coefficient of expansion to the interconnect substrate and the active devices (in our case GaAs). Although alumina has excellent low RF loss properties, its thermal conductivity is poor (-30 W/mK), Beryllia is often used for high power; however, aluminum nitride (AlN) has become preferable due to its non-toxic properties as well as compatibility of coefficient of thermal expansion with GaAs devices. Thermal conductivity of AIN (-260 W/mK) can be higher than that of aluminum (-200 W/mK) if made properly. From work which has been done in studying thermal fatigue of conductors on AIN microstrip lines for high frequency applications we have determined that bulk AIN is quite lossy compared to alumina for millimeter-wave frequencies [31]. This is mainly due to the high surface roughness. Ultra high-density AIN fabricated at JPL could only be polished down to 7μin and commercial samples have a surface roughness of about 3μin (only recently have commercial sources begin to achieve 1μin or better). Alumina. is typically <1μin. We have investigated a novel solution which involves the thin film deposition of high density AlN on alumina substrate. The AlN films are deposited using RF magnetron reactive sputtering of an Al target in the N_2/Ar gas mixture. The alumina substrate is polished and deposition conditions ensure that our film will have the same surface characteristics as the host substrate, This is a way to overcome high RF losses due to surface roughness. Initial thermal calculations show that a 10 μm thick film of AIN will have high enough thermal conductivity to keep a 0.5 W (20% power added efficiency) S SPA MMIC at a maximum junction temperature of 110°C. Junction temperatures of GaAs MESFETs on the SSPA MMIC chip as a function of thin film heat spreading layer thickness were calculated for aluminum nitride, copper, and diamond in Figure 6. As a part of our effort we developed both thin film copper and AIN on alumina processes for thermal spreader applications [31] . Although the thermal conductivity of AIN is lower, its coefficient of thermal expansion is better matched to alumina thus making it more attractive than the copper or diamond-like films.   In the future, other material systems such as diamond thin films can be considered. The structural substrate itself may be a diamond-like material.

Microstrip lines were fabricated on AlN-coated alumina substrates and thermal cycled (-50°C to +125°C) in order to observe the effects of thermal fatigue of the conductor/substrate interface. After 135 thermal cycles, no degradation in insertion loss of the microstrip was observed. We used sputtered Cr/Au bilayers to fabricate microstriplines. Cr and Au films were deposited by RF magnetron sputtering in Ar gas. The thickness of the Cr layer was about 10 nm and the thickness of Au was 3.7 μm. The details of deposition and properties of Cr/Au bilayers are given in [31].

E. Package assembly

The next critical issue is the attachment of the interconnection substrates to the structural substrate. In order to allow for reworkability of devices, the substrates attachment should employ a high temperature process. Sintering at first looks appealing, however the temperature required in this process is above the evaporation point of gold (860°C) which is our ground plane metallization. Glass sealing is another possibility. The easiest solution we found was to use a very thin high-temperature nonconductive epoxy (in order to avoid short-circuiting the coupling apertures), although outgassing of the epoxy is a concern for space applications.

Incorporating DC bias and control lines, although electrical in nature, becomes largely a materials problem. One approach is to use filled vias through the substrate. Metallized vias in alumina substrates have been successfully demonstrated using laser drilling techniques. For AIN there is less information. A variety of via sizes were laser drilled in commercially available thick AIN substrates, and some microcracks were observed. Further work should be done to evaluate the reliability of metal filled vias in these multilayer structures. A second alternative is to print the bias and control lines within the ground plane. Care must be taken **to avoid** DC short circuits while maintaining a continuous RF ground to a soldered lid. Glass-to-metal seals will provide electrical isolation, however difficulty arises in hermetically sealing the package. Due to limited financial resources, we did **not pursue this subject** in detail.

F. Hermeticity

Conventional hermetic electronic packages are usually sealed by soldering, brazing, laser welding, or seam sealing a lid over the contents of the package. We investigated a radically different approach in this area. A package would be sealed (but not hermetic) by soldering a cover to enclose the package, then a block copolymer coating (Teledyne TBC-P9632) would be painted onto it and cured at room temperature to achieve hermeticity. The coating has the viscosity of water and is easily removed, Areas that we don't want coated (e.g. where we want DC and ground plane continuity) can be masked off with paraffin and later removed. Our initial experiment was to take a standard Ku-Band commercial package, attach the lid with epoxy, and coat with the block copolymer coating, We used the MIL STD-883, method 1014 procedure to determine fine and gross leak properties. With a single coat, we achieved a fine leak rate of 10^{-7}/cc, however the package" failed the gross leak test. The gross leak failure was due to a degradation in the epoxy attachment of the lid. Two more tests were performed, under better controlled conditions. One package was sealed with epoxy, and one was sealed with solder. Both packages were coated with three layers of block copolymer material and both failed fine leak tests. The packages were then . thermal cycled and leak tested again, Hermeticity of the soldered package improved, passing fme and gross leak tests after 100 thermal cycles (-55° to 75°C). Therefore, the simple sealing techniques and. thermal curing of the block copolymer coating may be an alternative method of achieving hermeticity. More work should be done in this area.

111. Novel Applications

The basic package structure presented in Section II was for a simple drop-in application where both input and output embedding networks were microstrip. However, this approach can be used with many other printed structures and transmission line types, For example, the rnicrostrip patterns on the top side of the structural substrate can be printed probes for a waveguide to microstrip transitions (see Figure 7). In this application we can achieve a simple hermetic component within a single drop-in package. The next logical use is to incorporate an antenna as part of the top structural substrate pattern (e.g. for patch antennas, or even non-planar structures such as miniature horns).

The package itself may be considered as a 1:1 transformer. Based on this interpretation we can investigate new methods of matching into low and high impedance devices from the package level versus at the chip level (take advantage of level 2 packaging).

The real advantage of high density packaging is for the incorporation of many chips to comprise a MCM. This leads to N-port-capability which is achieved by the use of multiple planar and 3D input/output transitions. With the existence of multiple ports and high density of circuitry, the package architecture can be modified to include septums to provide higher levels of isolation for special applications,

In addition to the aforementioned features, optical interconnects for advanced system may be explored via a fiber transition or employing transparent or focusing structures as part of the structural substrate and/or package lid.

Iv. Conclusion

We have successfully investigated the key features of a new millimeter-wave package architecture, employed full wave 3-D electromagnetic modeling to design efficient wideband package transitions, developed new material techniques to address the thermal management issues, and initiated the investigation of a unique approach to achieve hermeticity. We have shown both theoretically and experimentally that millimeter-wave vertical interconnects are feasible with extremely low insertion loss and that the wideband characteristics solve the tolerance problem which drives up the cost of making millimeter-wave packages. New thin film multimaterial substrate systems provide high thermal conductivity in comparison to alumina while having a coefficient of thermal expansion close to that of GaAs. This approach allows us to take advantage of excellent surface smoothness (therefore, low loss) material properties of alumina. Finally, we have described unique applications of this package architecture which go beyond the traditional use of protecting a device. The package itself can be employed as part of a matching circuit, waveguide transition, antenna feed and even an antenna itself. One can go further to make it compatible with photonic networks.

We focused our efforts and limited financial resources in the analysis and demonstration of the critical features for this novel package since a final package geometry is a user defined quantity. This work was performed with the intent of providing a path towards affordable millimeter-wave packages which industry can adopt.

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5. Measurement and model (using FDTD techniques) of a back-to-back transition, Both the structural and interconnection substrates are on 10 mil alumina and the total length was 1 inch long. We normalized for comparison to a measured 1 inch long microstrip line. The insertion loss is less than 0.7 db (for two transitions) over 10 GHz and the return loss was better than 20 dB, Fixture mismatch at the higher frequency end degrades the comparison.
6. Simulation of the junction temperature of a 0.5W MMIC on an alumina substrate with various thickness of thin film heat spreaders, Although the AIN does not gives the lowest junction temperature it is closely matched in coefficient of thermal expansion making it a viable for packaging GaAs devices and MMICs. We have successfully developed techniques to deposit 10pm thin film AlN on polished alumina substrates.
7. This new package architecture can be employed for additional functionality beyond device protection. (a)Waveguide probe transition is incorporated as part of the structural substrate. This allows for a complete component to be "dropped" into a waveguide system. (b) Novel planar antenna feeds, etc. can be incorporated into the structural substrate thereby increasing modularity and saving in component cost(c) Optical signal can be incorporated into this packaging architecture via the structural substrate, a window in the package lid or via a fiber transition (only the window in the lid is shown).

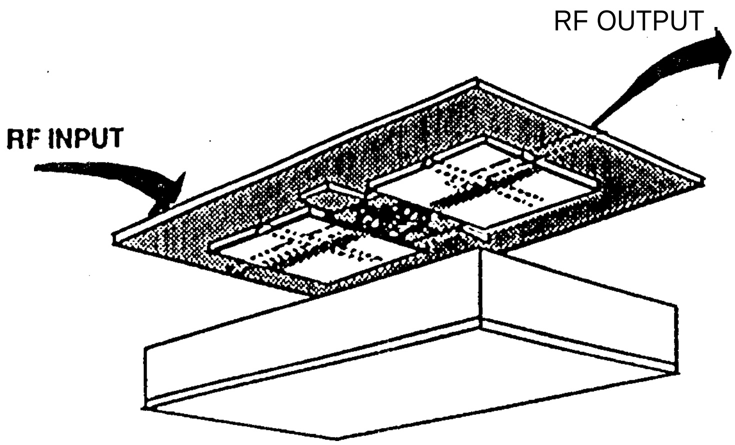
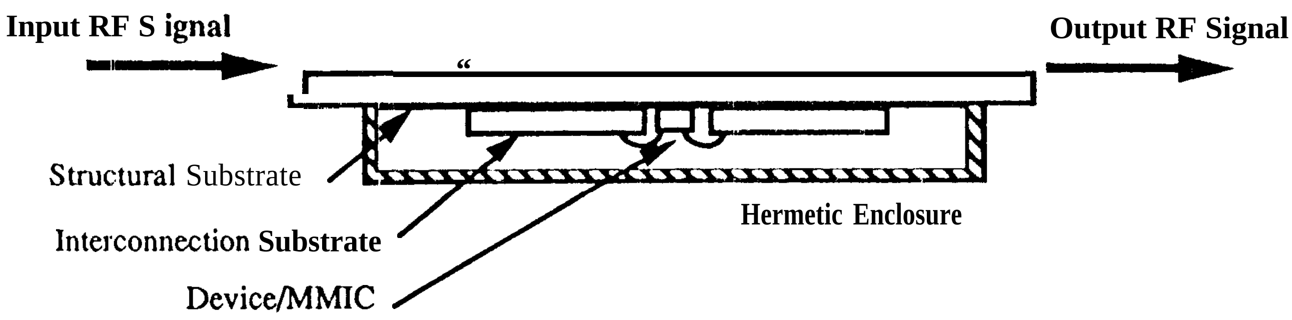


Figure 1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Output RF Signal
“
Structural Substrate
Interconnection Substrate
Device/MMIC
Hermetic Enclosure

Figure 2a

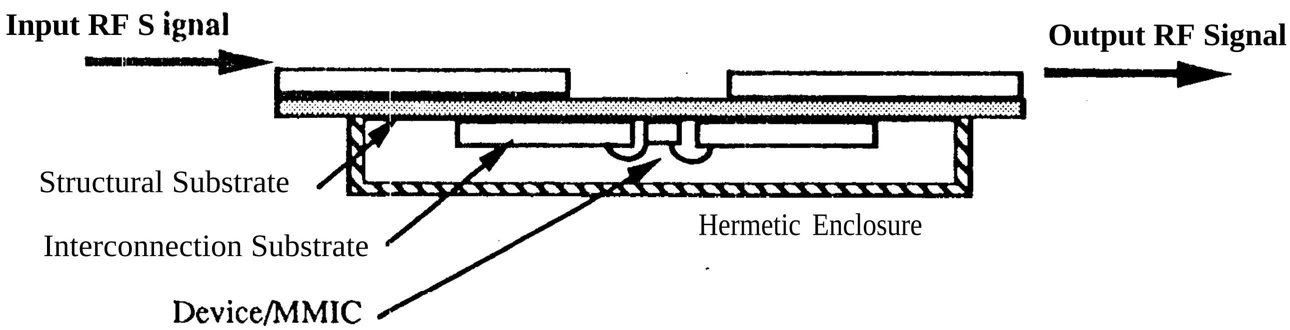

Input RF S ignal
Output RF Signal
Structural Substrate
Interconnection Substrate
Device/MMIC
Hermetic Enclosure

Figure 2b

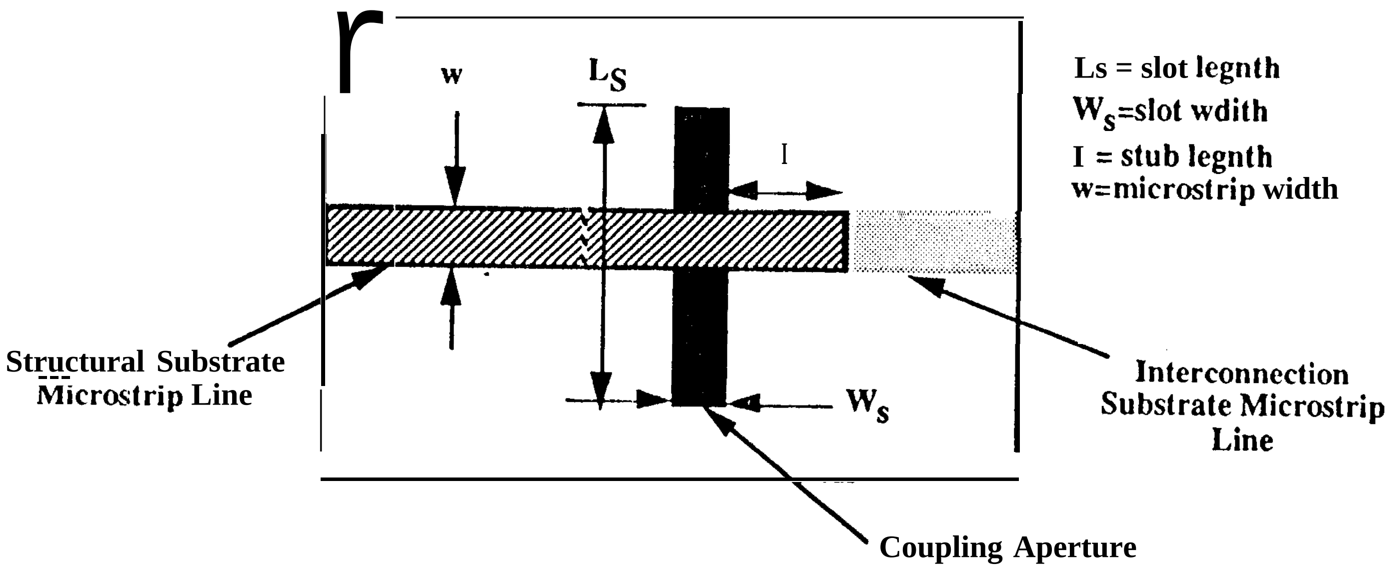
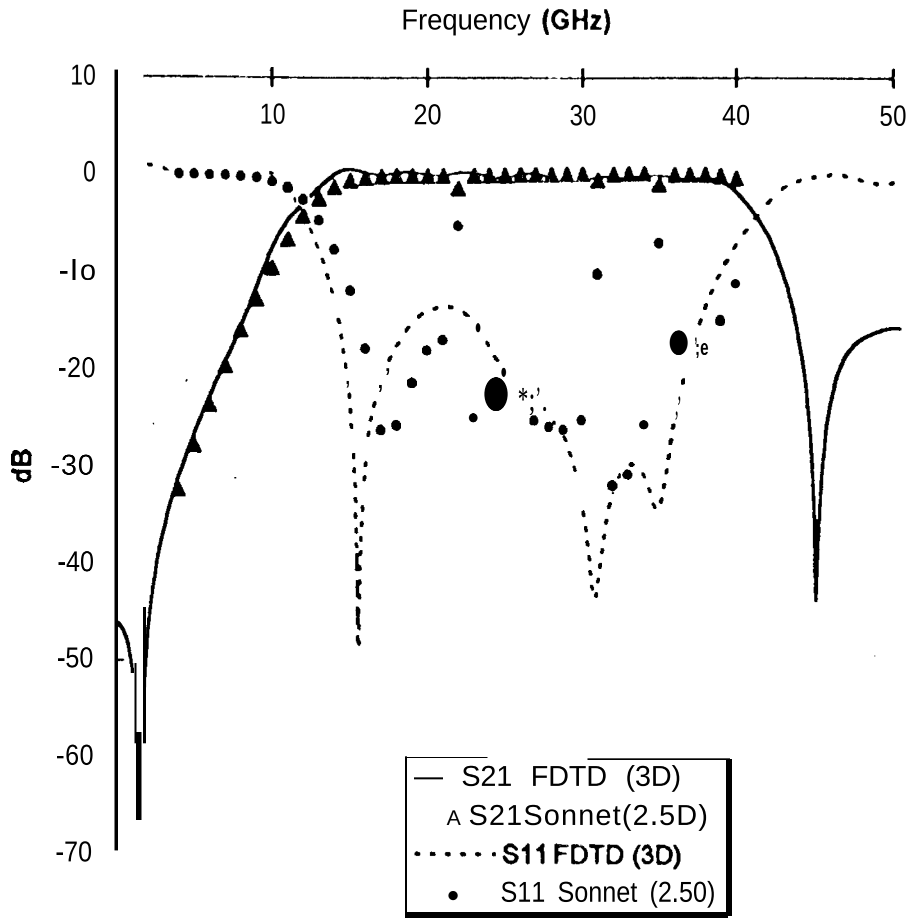
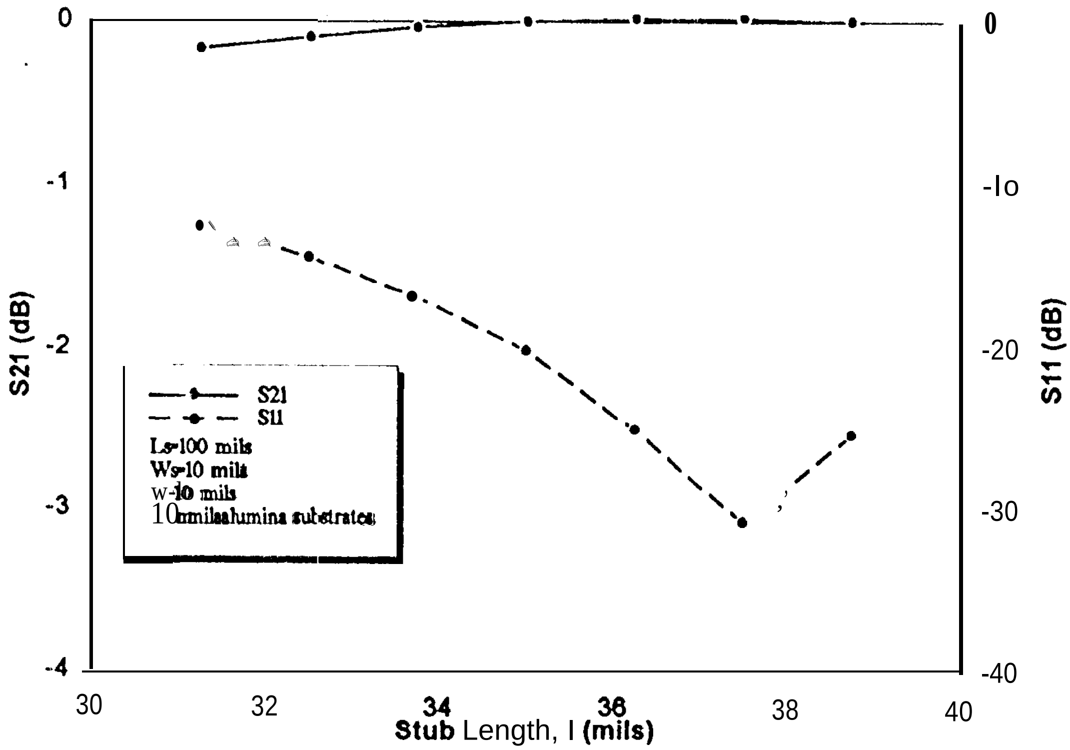

Ls = slot legnth
Ws=slot wdith
I = stub legnth
w=microstrip width
w
LS
I
Structural Substrate Microstrip Line
WS
Interconnection Substrate Microstrip Line
Coupling Aperture

Figure 2c



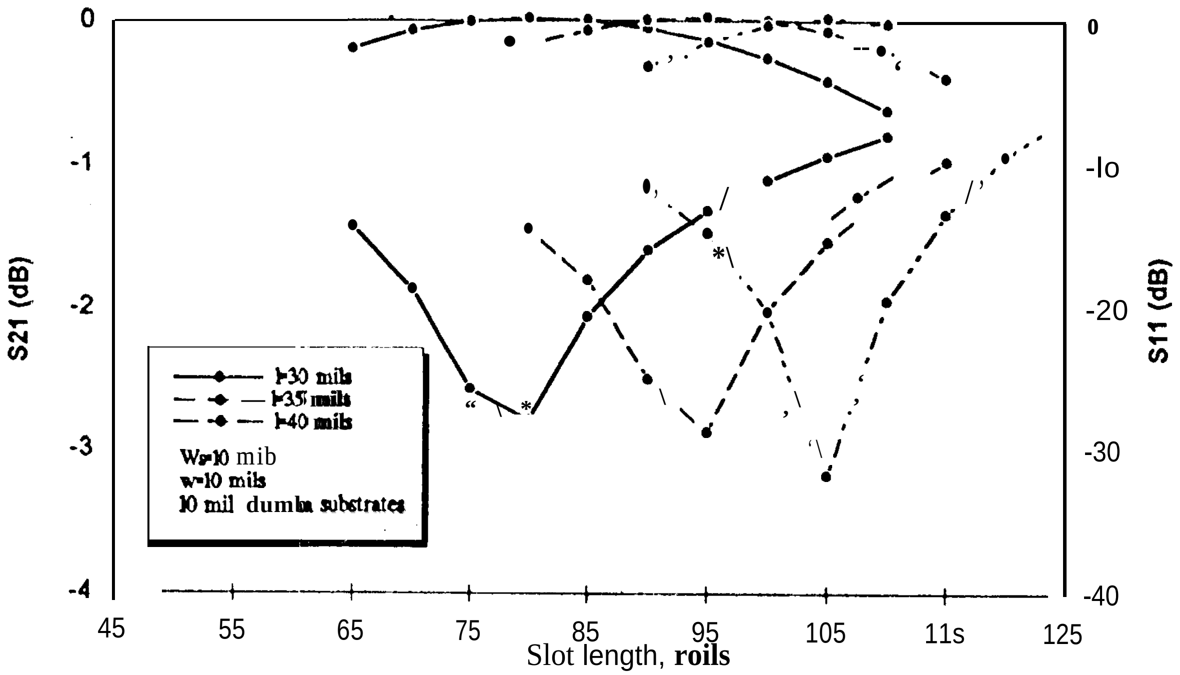
Frequency (GHz)
10
20
30
40
50
10
0
-lo
-20
-30
-40
-50
-60
-70
dB
— S21 FDTD (3D)
A S21Sonnet(2.5D)
S11 FDTD (3D)
S11 Sonnet (2.50)

Figure 3



0
-1
-2
-3
-4
S21 (dB)
S21
S11
Ls-100 mils
Ws-10 mils
w-10 mils
10 mils alumina substrates
0
-10
-20
-30
-40
S11 (dB)
30
32
34
36
38
40
Stub Length, l (mils)

Figure 4a



S21 (dB)
S11 (dB)
0
-1
-2
-3
-4
0
-lo
-20
-30
-40
45
55
65
75
85
95
105
11s
125
Slot length, roils
l=30 mils
l=35 mils
l=40 mils
Ws=10 mib
w=10 mils
10 mil dumba substrates

Figure 4b

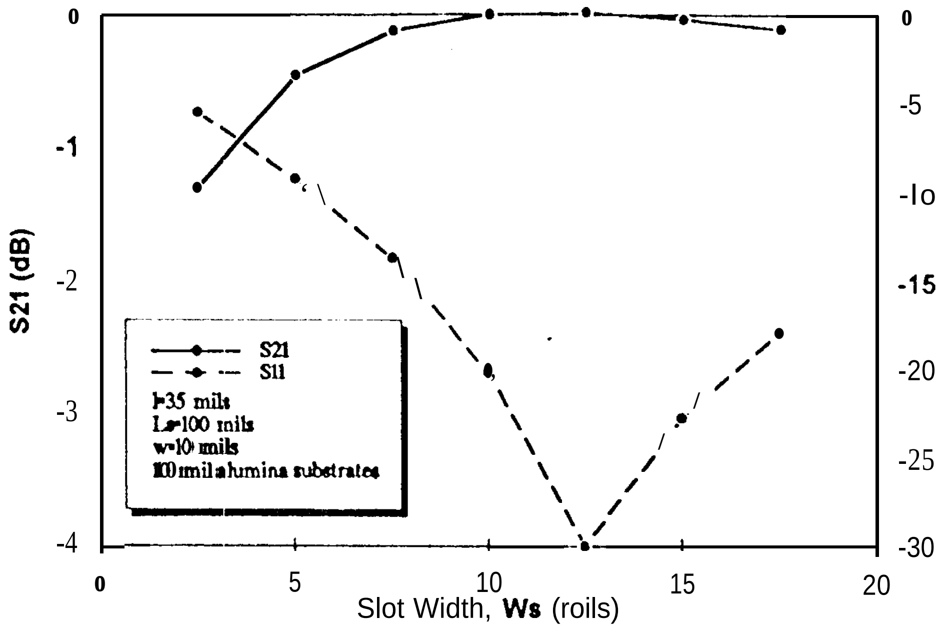

0
-1
-2
-3
-4
S21 (dB)
0
-5
-lo
-15
-20
-25
-30
S11 (dB)
S21
S11
l=35 mils
Ls=100 mils
w=10 mils
100 mil alumina substrates
0
5
10
15
20
Slot Width, Ws (roils)

Figure 4c

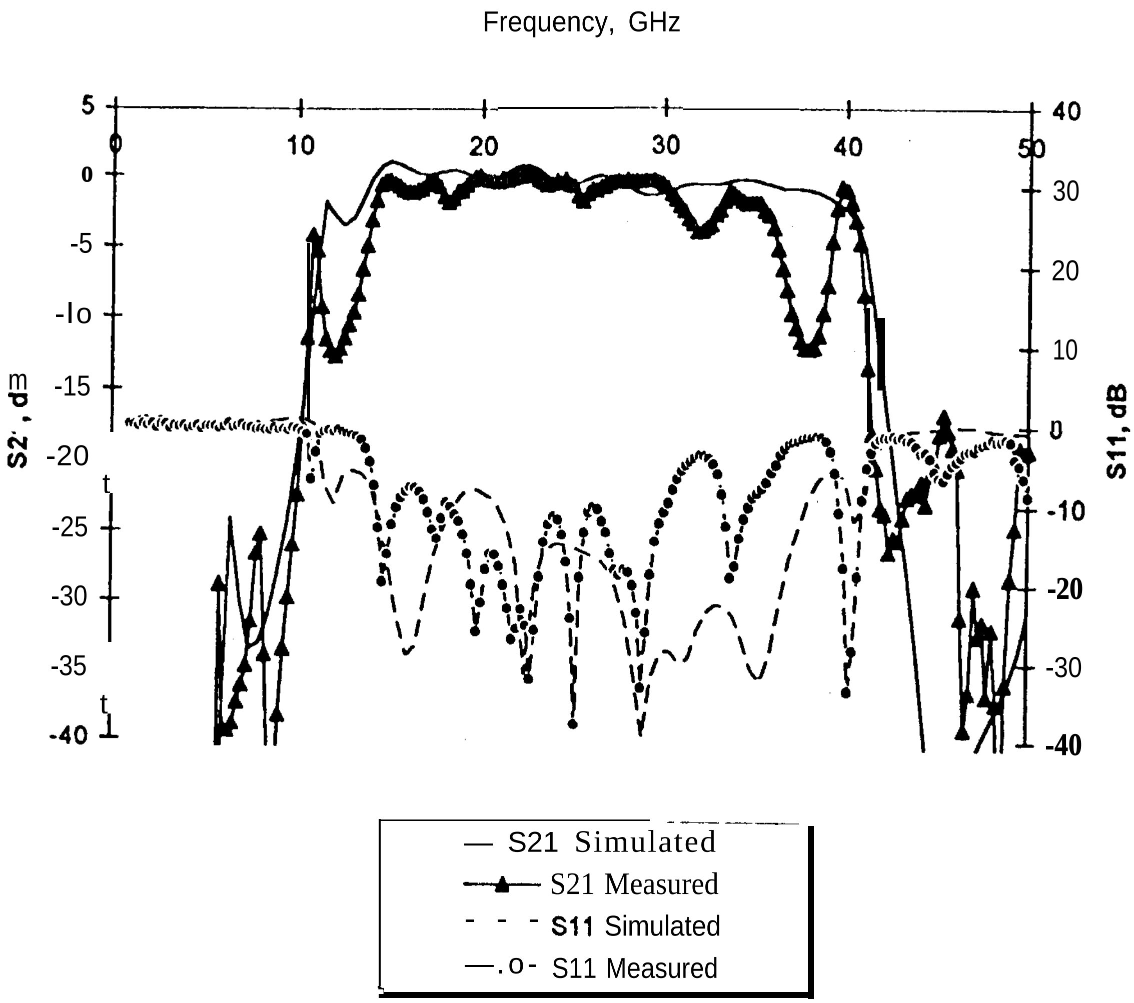

Frequency, GHz
5
0
-5
-lo
-15
-20
-25
-30
-35
-40
0
10
20
30
40
50
40
30
20
10
0
-10
-20
-30
-40
S2 , dm
S11, dB
— S21 Simulated
S21 Measured
- - - S11 Simulated
—.o- S11 Measured

Figure S

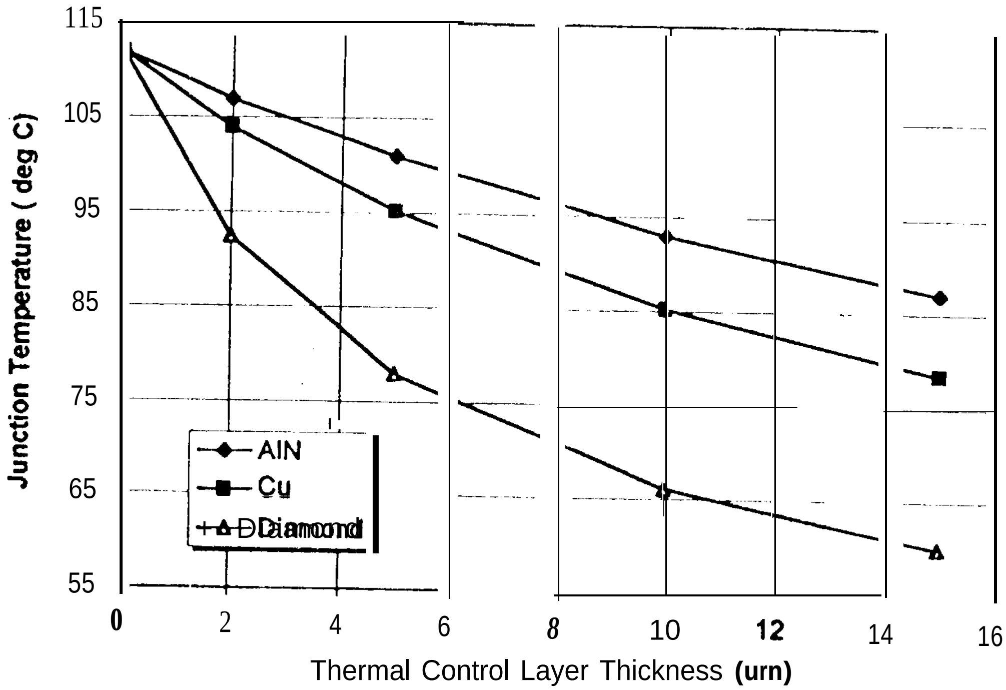

115
105
95
85
75
65
55
Junction Temperature (deg C)
AlN
Cu
Diamond
0
2
4
6
8
10
12
14
16
Thermal Control Layer Thickness (urn)

Figure 6

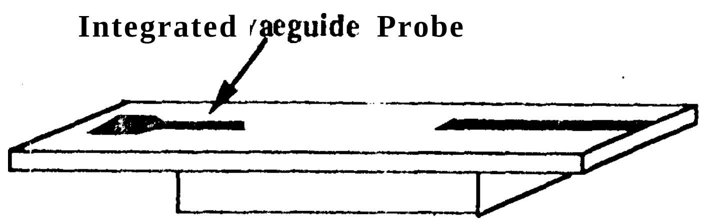


Figure 7a

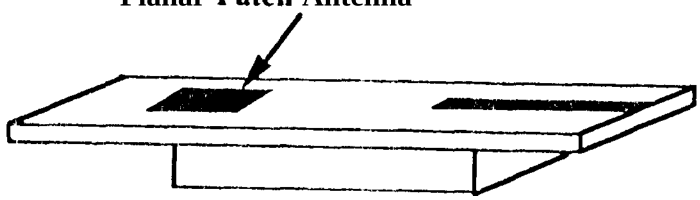


Figure 7b

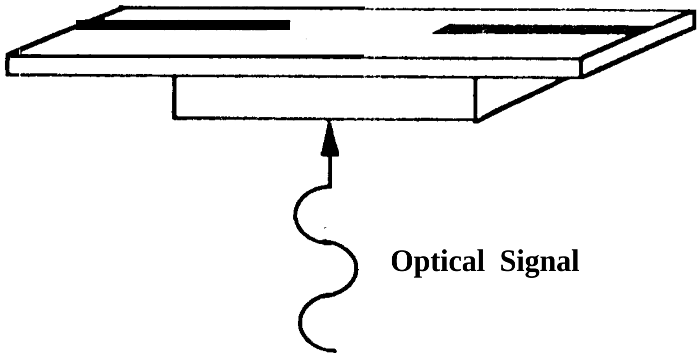


Figure 7c